***TEVFIK OZGU***

***150180082***

***a-) Draw the truth table for the Circuit a.***

***X C Overflow***

*0 0 0 0 0 0 0*

*0 0 0 1 0 Φ 1*

*0 0 1 0 1 1 0*

*0 0 1 1 1 0 0*

*0 1 0 0 1 0 0*

*0 1 0 1 1 1 0*

*0 1 1 0 0 1 0*

*0 1 1 1 0 Φ 1*

*1 0 0 0 1 1 0*

*1 0 0 1 1 0 0*

*1 0 1 0 0 0 0*

*1 0 1 1 0 Φ 1*

*1 1 0 0 0 1 0*

*1 1 0 1 0 Φ 1*

*1 1 1 0 1 0 0*

*1 1 1 1 1 1 0*

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***Write the simplest expression for the outputs Op, Sign, and Overflow.***

***Karnaugh Map Of :***

***X 00 01 11 10***

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | *1* | *1* |
| *1* | *1* |  |  |
|  |  | *1* | *1* |
| *1* | *1* |  |  |

***00***

***01***

***11***

***X***

***10***

*C*

***Simplest Expression of is X + X + X + X.***

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***Karnaugh Map Of :***

***X 00 01 11 10***

|  |  |  |  |
| --- | --- | --- | --- |
|  | *Φ* |  | *1* |
|  | *1* | *Φ* | *1* |
| *1* | *Φ* | *1* |  |
| *1* |  | *Φ* |  |

***00***

***01***

***11***

***X***

***10***

***C***

***Simplest Expression of Sign is X + X + C.***

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***150180082***

***Karnaugh Map Of :***

***X 00 01 11 10***

|  |  |  |  |
| --- | --- | --- | --- |
|  | *1* |  |  |
|  |  | *1* |  |
|  | *1* |  |  |
|  |  | *1* |  |

***00***

***01***

***11***

***X***

***10***

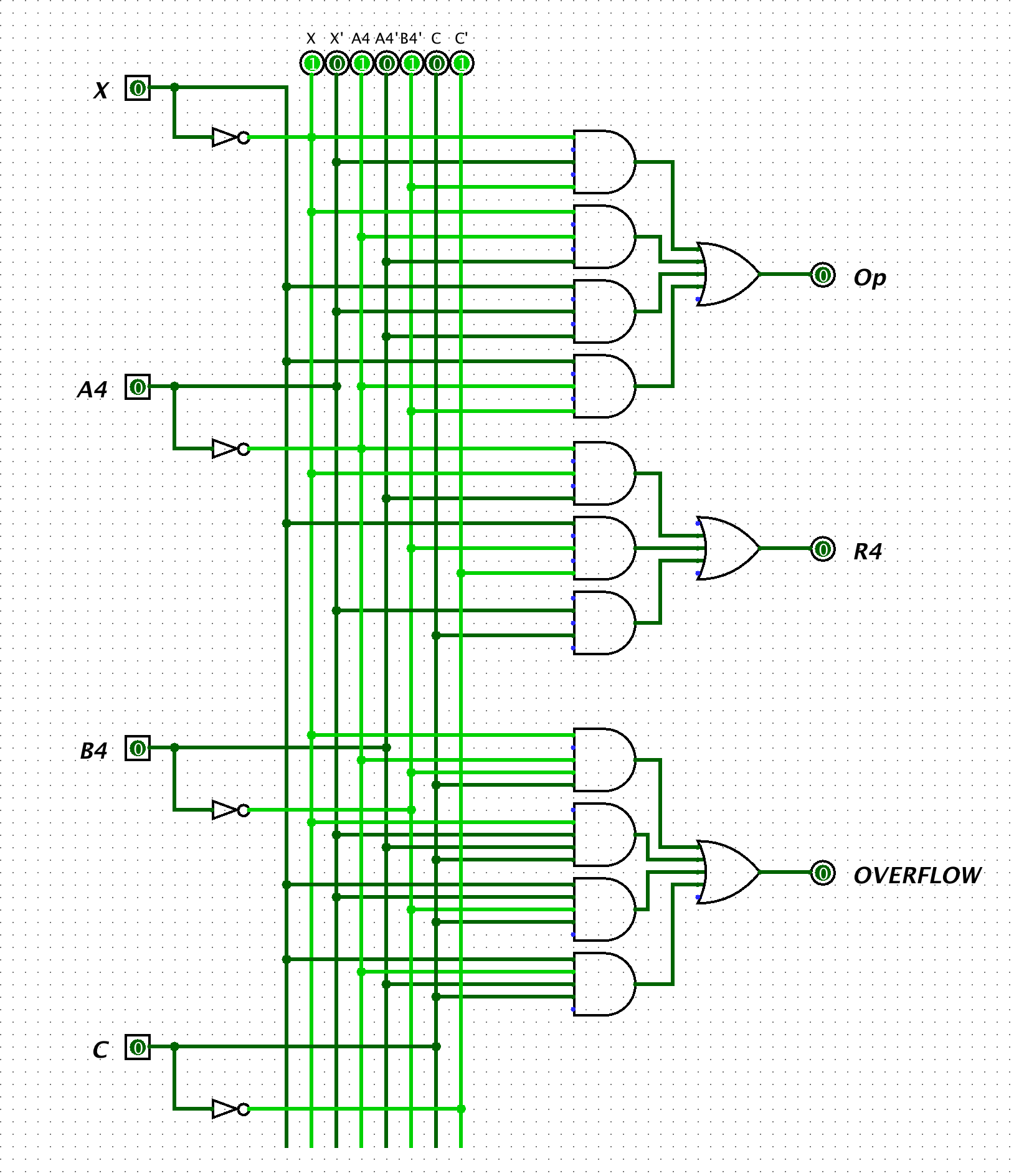
***C***

***Simplest Expression of Overflow is X + X +X+ X.***

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***150180082***

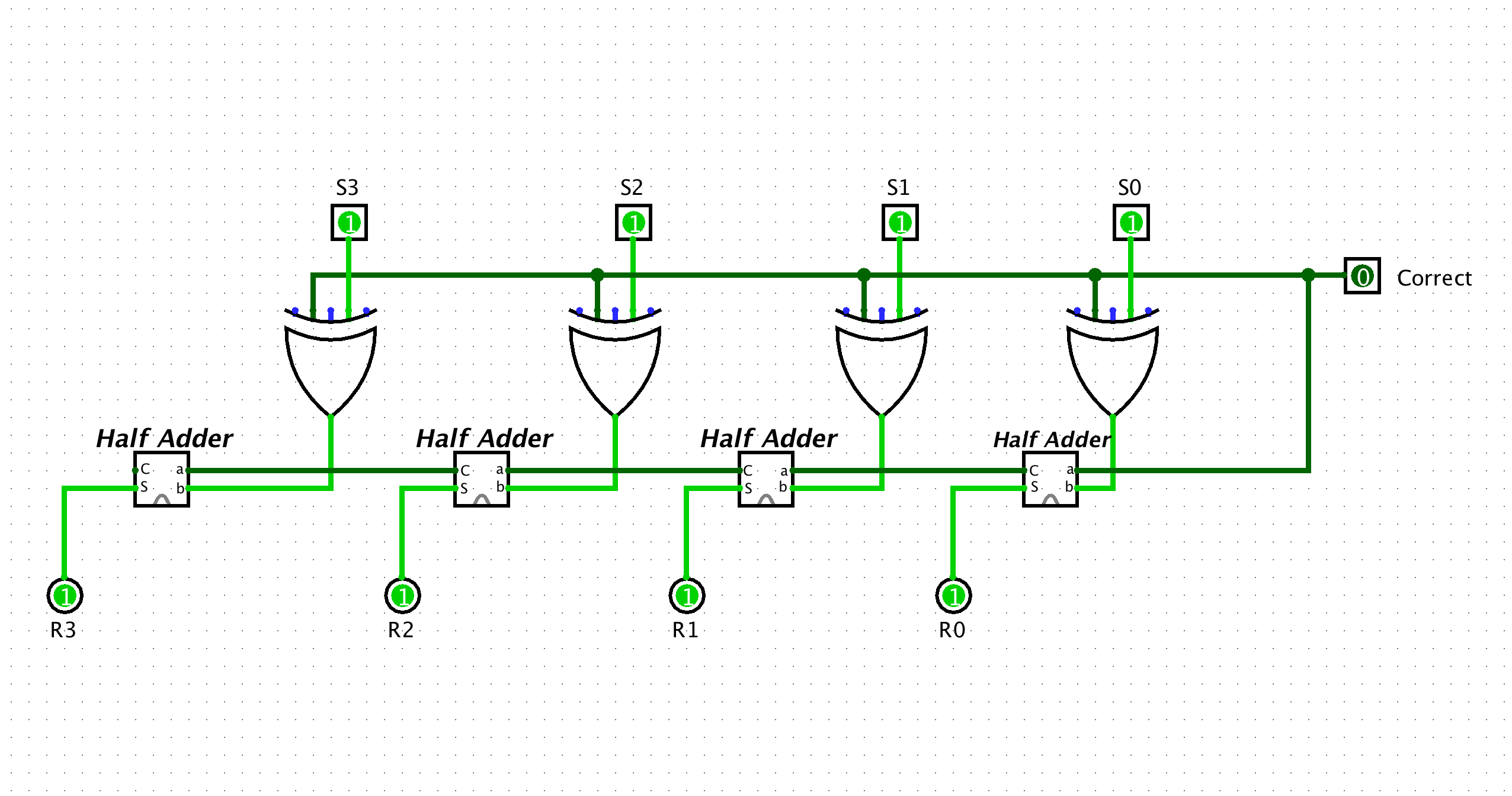
***Draw the circuit a using any type of logic gates. Fully label all input and outputs.***

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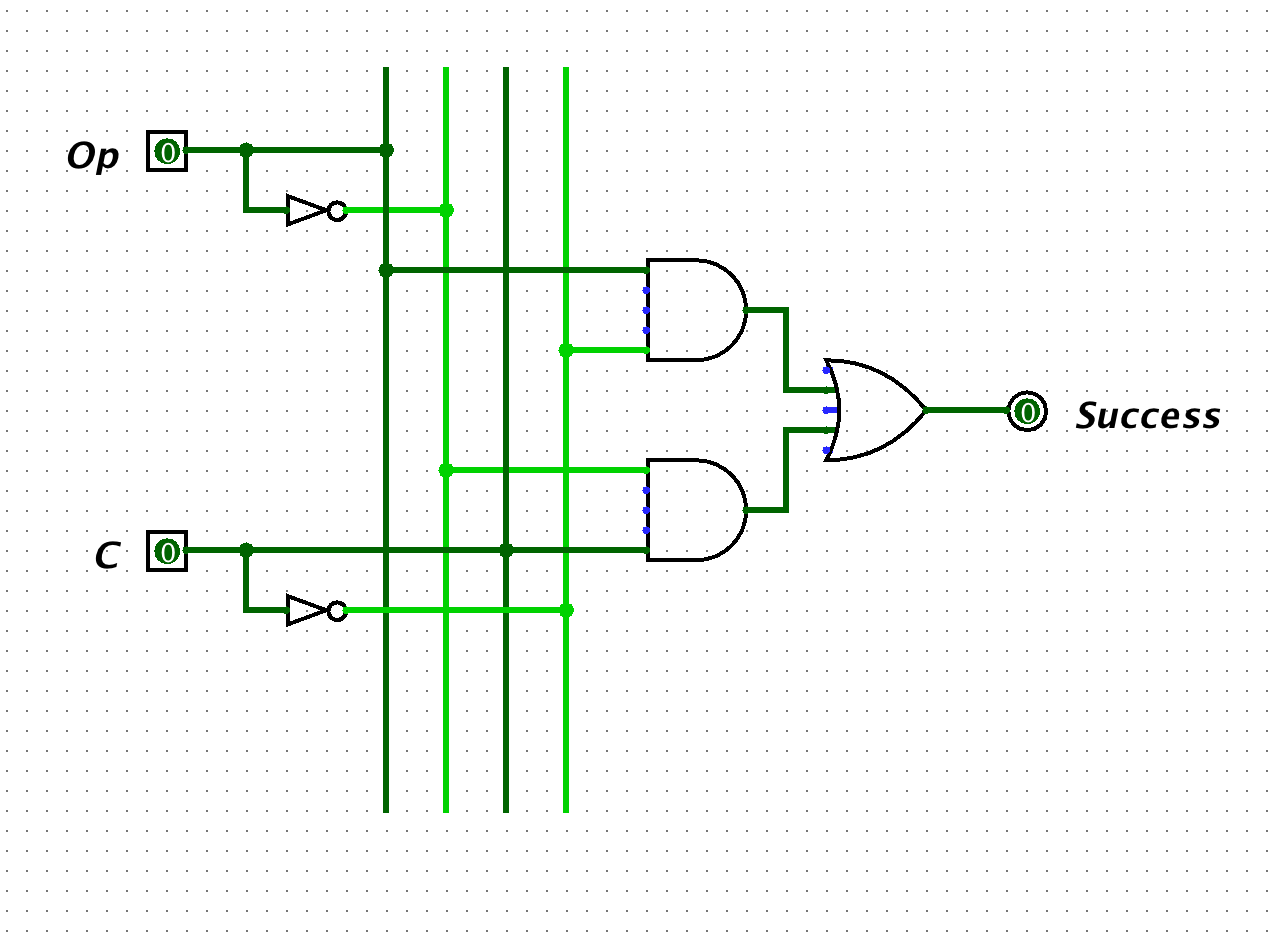
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***b)*** ***Design and draw the Circuit c using only half adders and minimum number of logic gates. Fully label all input and outputs.***

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***c) Design and draw the Circuit d using any type of logic gates. Fully label all input and outputs.***

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